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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	4303US (99-0584)
First Inventor or Application Identifier	Vernon M. Williams
Title	TRANSFER MOLDING AND UNDERFILLING METHOD AND APPARATUS
Express Mail Label No.	EL700255265US

JC936 U.S. PTO
09/652502
08/31/00

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)*
(Submit an original, and a duplicate for fee processing)

2. [X] Specification [Total Pages 28]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 7]

4. Oath or Declaration [Total Pages 1]
a. [ ] Newly executed (original or copy)
b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 17 completed)
[Note Box 5 below]
i. [ ] DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

5. [ ] Incorporation By Reference *(useable if Box 4b is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Microfiche Computer Program *(Appendix)*

7. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. [ ] Computer Readable Copy
b. [ ] Paper Copy (identical to computer copy)
c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
14. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s)
(if foreign priority is claimed)
16. [ ] Other: .....

** A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.*

17. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: _____/_____

Prior application information: Examiner _____ *Group / Art Unit:* _____

18. CORRESPONDENCE ADDRESS

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PATENT TRADEMARK OFFICE

Name (Print/Type)	Brick G. Power	Registration No. (Attorney/Agent)	38,581
Signature	Brick Power	Date	08/31/00

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FEE TRANSMITTAL for FY 2000

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Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12. See 37 C.F.R §§ 1.27 and 1.28.

TOTAL AMOUNT OF PAYMENT ($) 2328.00

Complete if Known	
Application Number	Not yet assigned
Filing Date	August 31, 2000
First Named Inventor	Vernon M. Williams
Examiner Name	Unknown
Group / Art Unit	Unknown
Attorney Docket No.	4303US (99-0584)

METHOD OF PAYMENT (check one)

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to.

Deposit Account Number: 20-1469

Deposit Account Name: Trask Britt

[X] Charge Any Additional Fee Required Under 37 CFR §§ 1.16 and 1.17

2. [X] **Payment Enclosed:**
[X] Check [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	690	201	345	Utility filing fee	690
106	310	206	155	Design filing fee	0
107	480	207	240	Plant filing fee	0
108	690	208	345	Reissue filing fee	0
114	150	214	75	Provisional filing fee	0

SUBTOTAL (1) ($) 690.00

2. EXTRA CLAIM FEES

		Extra Claims		Fee from below	Fee Paid
Total Claims	98 -20** =	78	X	18	= 1404
Independent Claims	6 - 3** =	3	X	78	= 234
Multiple Dependent				0	= 0

**or number previously paid, if greater; For Reissues, see below

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	260	204	130	Multiple dependent claim, if not paid
109	78	209	39	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 1,638.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	380	216	190	Extension for reply within second month	
117	870	217	435	Extension for reply within third month	
118	1,360	218	680	Extension for reply within fourth month	
128	1,850	228	925	Extension for reply within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing a brief in support of an appeal	
121	260	221	130	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,210	241	605	Petition to revive - unintentional	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	690	246	345	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	690	249	345	For each additional invention to be examined (37 CFR § 1.129(b))	

Other fee (specify) _____

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($)

SUBMITTED BY				Complete (if applicable)	
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Signature	Brick Power			Date	08/31/2000

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PATENT
Attorney Docket 4303US (99-0584)

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EL700255265US

Date of Deposit with USPS: August 31, 2000

Person making Deposit: Amanda Trulson

APPLICATION FOR LETTERS PATENT

for

TRANSFER MOLDING AND UNDERFILLING METHOD AND APPARATUS

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TRANSFER MOLDING AND UNDERFILLING METHOD AND APPARATUS

BACKGROUND OF THE INVENTION

Field of the Invention: The present invention relates method and apparatus used in transfer molding to providing a flowable resin to a substrate having one or more semiconductor devices thereon for the packaging thereof. More specifically, the present invention relates to a method and apparatus used in transfer molding to preventing voids and air pockets in a flowable resin provided to a substrate having one or more semiconductor devices thereon for the packaging thereof.

State of the Art: At present, transfer molding is a widely adopted method for plastic encapsulation of semiconductor devices. In transfer molding, the mold generally includes a lower half and an upper half. The lower half of the mold will typically include multiple cavities and a concave portion, called a pot, which communicates with the multiple cavities through runners. In one instance of molding a package, a lead frame at the outer periphery of a semiconductor device is placed on an edge of each of the cavities. The upper half of the mold is placed on the lower half of the mold and includes cavities and a through hole corresponding to the cavities and the pot of the lower half of the mold, respectively. The cavity of either the upper half or lower half, or both, includes a vent, usually at the opposite end of the cavity from the runner, to allow air to push therethrough. An assembly of a semiconductor device and a lead frame connected thereto is arranged in each space defined between corresponding cavities of the lower half and upper half of the mold, where each of the cavities are oriented longitudinally along the horizontal plane. A thermosetting resin is heated in the pot and fed therefrom by a plunger. The resin reaches the cavities through the runners and covers the semiconductor device and a portion of the lead frame located in each of the cavities, pushing air from the runners and cavities through the vent. The resin is typically then heated to cure the same, thus encapsulating the semiconductor device and adjacent portion of the lead frame.

However, as shown in drawing FIG. 1, when the resin 1 flows to fill the horizontally oriented cavities 3, the flow is usually not uniform due to various design

factors of the semiconductor device and lead frame and gravity acting on the resin 1. As a result, the fronts 1a, 1b of the resin 1 flowing above and below the semiconductor device 32 will often meet above the semiconductor device 32 instead of at the vent, causing the molded package to have undesirable air pockets and/or voids 2, as shown in drawing FIG. 2. These type of defects not only degrade the outer appearance of the molded package, but also produce reliability problems with respect to its resistance to thermal shock, and exposure to humidity and other contaminants.

In an effort to prevent such defects in the molded package, United States Patent 4,900,485 to Murakami discloses a method and apparatus for transfer molding semiconductor devices including a hydraulic pressure controller and a pressure detector to control the pressure of the resin therein. Additionally, other methods made to prevent defects such as voids by controlling the temperature of the resin are disclosed in United States Patent 4,908,178 to Nakagawa et al. and United States Patent 5,071,334 to Obara. Although each of the above references disclose a method and/or apparatus for limiting air pockets and/or voids in a molded package, each reference discloses a transfer mold that is longitudinally oriented to be horizontal. Thus, as previously discussed, there remains the problem of non-uniform flow fronts in the transfer mold, resulting in air pockets and/or voids.

Along with the previously discussed problems in transfer molding, methods in flip chip packaging are known to present similar problems of voids and/or air pockets in underfill material 1 in a gap between a bumped semiconductor die and a substrate. As shown in drawing FIG. 3, such methods include a one-sided or two-sided dispense process, where an underfill material, such as resin 1, is dispensed along one or two adjacent sides of the semiconductor die 52. The underfill resin 1 then freely flows by capillary action between the semiconductor die 52 and substrate 64, pushing air existing in the gap between the die 52 and the substrate from opposing sides of the semiconductor die 52 as the underfill material fills the gap, thereby minimizing potential voids. However, as shown in drawing FIG. 3, the underfill resin 1 will often leave air pockets or voids 2 adjacent the bumps 56 of the flip chip semiconductor die 52. Further, it is desirable to improve the time it takes to fill the gap with the underfill material.

United States Patent 5,766,982 to Akram et al. addresses improving the time for underfilling a flip-chip package by elevating the package on an inclined plane from a horizontal plane. In this method, the underfill material is dispensed either through an aperture in the substrate or at one or two elevated sides of the gap between the die and substrate. When dispensing the underfill material by these methods, the underfill material filling the gap flows down the inclined plane, thereby, utilizing gravity to decrease the time necessary for underfilling. Although this method improves the time for underfilling, there remains the potential for voids and air pockets to form due to non-uniform flow, and in particular, voids forming adjacent the bumps of the flip-chip package.

Therefore, it would be advantageous to obtain substantially uniform flow of a packaging or underfill resin to reduce or eliminate the occurrence of voids in the resin, as well as to provide molds and systems that facilitate uniform resin flow during packaging or underfill operations.

SUMMARY OF THE INVENTION

The present invention relates to a method and apparatus for limiting voids in a flowable packaging material provided to a substrate, such as a semiconductor die or a wafer or other large-scale substrate including a plurality of semiconductor devices fabricated thereon. The present invention is directed to a method and apparatus for providing the flowable material to the substrate in a substantially vertical direction with respect to a horizontal plane. The method of the present invention includes orienting the substrate substantially vertically.

In one embodiment, the present invention includes a transfer mold having at least one cavity with a gate at a lower portion of the cavity and a vent at an upper portion of the cavity, in which the cavity may be oriented longitudinally perpendicular to the horizontal plane and configured to vertically orient the substrate. According to this embodiment of the present invention, the flowable material fills the cavity from the gate at the bottom thereof to the vent at the top thereof to encapsulate the substrate and/or provide a layer of the flowable material over at least a portion of the substrate. By this

arrangement, voids and air pockets are substantially prevented from forming in the flowable material since the flowable packaging material fills the cavity in the vertical direction and due to the force of gravity acting on the flowable material.

In another embodiment, the present invention includes a semiconductor device attached to a substrate having bumps therebetween, in which the bumps provide a gap between the semiconductor device and the substrate. According to this embodiment of the present invention, the semiconductor device and substrate are oriented substantially vertically so that the gap may be filled with flowable underfill material in a vertical direction. This embodiment may include a barrier positioned about the periphery of the semiconductor device for containing the flowable material in the gap between the semiconductor device and the substrate. The barrier includes an opening where the flowable material is introduced into the gap. The flowable material fills the gap from the bottom thereof and is drawn upwardly therethrough by way of capillary action or under positive or negative pressure.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

The method and apparatus of the present invention will be more fully understood from the detailed description of the invention taken in conjunction with the drawings, wherein:

FIG. 1 is cross-sectional side view of a conventional transfer molding process, depicting flowable thermoset resin being transferred into a mold cavity with a semiconductor device therein;

FIG. 2 is a cross-sectional side view of the conventional transfer molding process of FIG. 1, depicting an encapsulated semiconductor device in a mold cavity having a void in the molded resin;

FIG. 3 is a cross-sectional top view of an assembly, including a semiconductor die flip chip bonded to a carrier substrate, depicting underfill material being dispensed between the semiconductor die and the substrate and voids forming adjacent the solder bumps in a conventional underfill process;

FIG. 4 is a cross-sectional side view of a semiconductor device in a vertically oriented mold cavity, illustrating resin encapsulating the semiconductor device so that the resin fills the cavity in a substantially vertical upward direction, in accordance with the present invention;

FIG. 5 is a cross-sectional side view of a substrate in a vertically oriented cavity, illustrating resin flowing in the vertically oriented cavity in a substantially vertical upward direction, in accordance with the present invention;

FIG. 6 is a cross-sectional side view of a substrate in a vertically oriented cavity, wherein the cavity includes protrusions configured to contact bond pads or contacts of the substrate, and illustrating resin flowing into the vertically oriented cavity in a substantially vertical upward direction, in accordance with the present invention;

FIG. 7 is a cross-sectional side view of a ball grid array substrate positioned in a vertically oriented cavity, illustrating resin flowing upwardly into the vertically oriented cavity, in accordance with the present invention;

FIG. 8 is a cross-sectional side view of an assembly, including a carrier substrate and a semiconductor device flip chip bonded thereto, in a vertically oriented cavity, illustrating resin flowing in the vertically oriented cavity in a substantially vertical upward direction, in accordance with the present invention;

FIG. 9 is a cross-sectional side view of an assembly of a carrier substrate and a semiconductor device flip chip bonded thereto, illustrating an underfill process between the semiconductor device and substrate in a substantially vertical upward direction, in accordance with the present invention; and

FIG. 10 is a cross-sectional front view taken along line 10--10 of drawing FIG. 9, illustrating the underfill process in the vertically oriented direction, in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Embodiments of the present invention will be hereinafter described with reference to the accompanying drawings. It should be understood that the illustrations are not meant to be actual views of any particular apparatus and/or method, but are merely idealized representations which are employed to more clearly and fully depict the present invention than would otherwise be possible. Additionally, elements common between the figures retain the same numerical designation.

A first embodiment of the present invention is illustrated in drawing FIG. 4, depicting a transfer mold 5 for encapsulating an assembly 31 of a semiconductor device 32 and an adjacent portion of a lead frame 33 connected thereto by utilizing a transfer molding process. The term "transfer" molding is descriptive of this process as the molding compound, in a liquid state, is transferred by capillary action or under pressure to a plurality of remotely-located mold cavities 10 containing semiconductor device assemblies 31 to be encapsulated.

The transfer mold 5 includes a first half 12 and a second half 14 which form a plurality of cavities 10 therebetween. However, for purposes of simplicity, only one cavity 10 is illustrated in drawing FIG. 4. The cavity 10 includes a gate 16 and a vent 20. The gate 16 is used as an inlet for resin 24 to flow into the cavity 10. The vent 20, located at an opposite end of the cavity 10 from the gate 16, permits air or other gases in the cavity 10 to escape therefrom upon introduction of resin 24 into the cavity 10.

As known to those skilled in the art of transfer molding, a pellet preferably containing liquid thermoset resin mold compound, which is also referred to herein as resin 24 for simplicity, is disposed above a plunger in a pot (not shown). The plunger engages and melts the pellet, forcing the liquid resin 24 that was contained therein through a sprue to runners which each lead to the plurality of cavities. As shown in drawing FIG. 4, each runner 18 leads to the gate 16 of a cavity 10, allowing the resin 24 to fill the cavity 10 and encapsulate the semiconductor device 32 and the adjacent therein.

In the present invention, the vent 20 is located substantially at an upper portion 4 of the cavity 10 with the gate 16 preferably located at a lower portion 6 of the cavity 10.

In particular, as shown in drawing FIG. 4, it is preferable that the mold cavity 10 be oriented substantially vertical and longitudinal along a vertical plane 30 which is substantially perpendicular or at substantially ninety (90°) from a horizontal plane 28. As such, when the resin 24 fills the cavity 10, the flow fronts 26 and 26′ rise vertically toward the vent 20 at substantially the upper portion 4 of the cavity 10. Further, the flow fronts 26 and 26′ rise substantially at the same rate due to the force of gravity acting on the flow fronts 26 and 26′. Therefore, gravity helps control the flow fronts 26 and 26′ to equalize and become substantially one flow front prior to reaching the vent 20 at the upper most portion 4 in the cavity 10, allowing the resin 24 to substantially fill all portions of the cavity 10 and forcing air or gases within the cavity 10 through the vent 20 without substantially creating air pockets and/or voids in resin 24. Even if the flow fronts 26 and 26′ rise at different rates prior to surpassing an edge 34 of the semiconductor device 32, the flow fronts 26 and 26′ will substantially equalize each other after reaching the uppermost edge 34 of the semiconductor device 32 due to the force of gravity acting thereon. In this manner, gravity provides a more uniform flow front, wherein gravitational force induces the filling of spaces where potential air pockets and/or voids were conventionally formed in the cavity 10. Therefore, the present invention substantially prevents the conventional problems of voids and air pockets as previously discussed. In the present invention, the fluid molding material is caused to flow over any desired substrate having any type and number of semiconductor devices attached thereto in a substantially vertical direction, such as a substrate and semiconductor device(s) being located in the mold cavity at approximately ninety degrees (90°) with respect to the horizontal axis of the mold cavity.

According to the first embodiment of the present invention, the semiconductor device is preferably a lead frame packaging assembly utilizing wire bonding, tape automated bonding (TAB), and/or any known bonding technique from the semiconductor device to leads of the lead frame as known in the art. However, the present invention is not limited to lead frame packaging assemblies, but may also encompass transfer molding of semiconductor assemblies including semiconductor devices secured to other carriers, such as carrier substrates or interposers, by way of wire bonds, tape automated bonds

(TAB), flip chip bonds, or other known techniques. Alternatively, the methods and apparatus of the present invention may be used to package or form protective layers on individual semiconductor device components (e.g., semiconductor dice, interposers, carrier substrates, other carriers, etc.). In addition, the semiconductor device in the present invention is preferably vertically oriented, substantially perpendicular to the horizontal plane 28. However, the semiconductor device 32 may be oriented at any inclined angle from the horizontal plane 28, so long as the force of gravity creates a uniform flow front that will permit substantially all of the air or other gases within the cavity 10 to escape therefrom so as to reduce or eliminate the formation of voids or air pockets in resin 24.

A second embodiment of the present invention is illustrated in drawing FIG. 5, depicting resin 24 filling a transfer mold 5′ in a substantially vertical direction similar to that of the first embodiment. However, instead of a semiconductor device being encapsulated as in the first embodiment, the second embodiment comprises a first surface 44, or back side, of a substrate 42, such as an individual semiconductor die or a wafer or other large scale substrate with a plurality of semiconductor devices thereon, abutting a first half 12′ of the cavity 10′, which is configured to retain substrate 42. Further, there may be multiple substrates 42 within a single cavity 10′. The other, active, surface 45 of the substrate 42 is exposed to the remainder of the cavity 10′. As the resin 24 vertically rises in the cavity 10′, the resin 24 covers at least surface 45 of the substrate 42 and may cover other surfaces of the substrate, depending on how the substrate 42 is situated within the cavity 10′. The substrate 42 is preferably substantially vertically oriented relative to a horizontal plane 28. However, the plane of the substrate 42 may be oriented at any inclined angle from the horizontal plane 28, so long as the vent 20′ in the cavity 10′ is substantially at the upper portion 4 of the cavity 10′ and the force of gravity acting on the resin 24 will continue to force substantially all air or other gases out of the cavity through the vent 20′ before any air pockets or other voids form. Following such encapsulation, bond pads on surface 45 may be exposed through the cured resin 24 by known techniques, such as mask and etch processes.

A third embodiment of the present invention is illustrated in drawing FIG. 6, depicting resin 24 filling a transfer mold 5″ in a substantially vertical direction to cover at least a portion of the second surface 45 of the substrate 42. The fourth embodiment is similar to the second embodiment in all respects, except the second half 14″ of the transfer mold 5″ includes a plurality of projections 50 configured to extend to the surface 45 of the substrate 42 and contact bond pads 47 thereon. The projections 50 extending from the second half 14″ of the transfer mold 5″ allow resin 24 to rise vertically around the projections 50. Thus, bond pads 47 on the second surface 45 of the substrate 42 that are contacted by projections 50 are shielded from resin 24 and are free of resin 24. Therefore, the resin-free bond pads 47 of the substrate 42 can receive solder balls or the like without further significant modification of the layer of resin 24 on surface 45. Moreover, the openings formed in resin 24 may define the configurations of at least the lower portions of solder bumps or other conductive structures formed on bond pads 47.

A fourth embodiment of the present invention is illustrated in drawing FIG. 7, depicting resin 24 filling the cavity 10‴ of a transfer mold 5‴ in a substantially vertical direction to cover at least the second surface 55 of the substrate, in this case a flip chip type semiconductor die 52. Of course, the cavity 10‴ may alternatively be configured to hold and facilitate encapsulation of an individual semiconductor die 52, a plurality of individual dice, or a wafer or other large-scale substrate with a plurality of semiconductor devices thereon. The third embodiment is similar to the second embodiment in all respects, except the semiconductor die 52 includes conductive structures 56, such as balls, bumps, pillars, or columns including a conductive material such as a solder, other metal or metal alloy, a conductive epoxy, a conductor-filled epoxy, or a z-axis conductive elastomer, predisposed on and protruding from the bond pads thereof. Additionally, the second half 14‴ of the transfer mold 5‴ may include a plurality of recesses 58 formed in the and configured to receive portions of conductive structures 56 so as to prevent resin 24 from completely covering same.

A fifth embodiment of the present invention is illustrated in drawing FIG. 8, depicting resin 24 filling a transfer mold 105 in a substantially vertical direction. The

fifth embodiment is similar to the second embodiment in all respects, except the cavity 110 is configured to receive and at least partially encapsulate a flip-chip assembly 62. The flip-chip assembly 62 includes a carrier, such as a carrier substrate 64 or an interposer, and a flip chip type semiconductor die 52 with conductive structures 66. As such, the conductive structures 66 connected to carrier substrate 64 provide electrical connection and a gap 72 between an active surface of the semiconductor die 52 (i.e., the surface facing substrate 64) and the substrate 64. In the fifth embodiment, there may also be a space 74 between the surface of the second half 114 of the transfer mold 105 and back side 57 of the semiconductor die 52. Alternatively, the back side 57 of the semiconductor die 52 may abut with the inside surface of the second half 114 of the transfer mold 105. Furthermore, in the fifth embodiment of the present invention, the resin 24 has a viscosity that allows optimal underfilling of the gap 72, as known in the art. Thus, it can be well appreciated that by controlling the viscosity of the resin 24, underfilling may be accomplished efficiently while also preventing air pockets and/or voids in the gap 72, in accordance with the present invention.

In addition, as in the previous embodiments, the flip-chip assembly 62 is preferably oriented substantially vertically relative to a horizontal plane 28. However, the assembly 62 may be oriented at any inclined angle from the horizontal plane 28, so long as the vent 120 in the cavity 110 that the flip-chip assembly 62 sits within is substantially at the upper portion 104 of the cavity 110 and the force of gravity acting on the resin 24 continues to force substantially all of the air or other gases out of the cavity through the vent 120 before any air pockets or other voids form.

A sixth embodiment is illustrated in drawing FIG's. 9 and 10, depicting resin 24 filling a gap 72 between a semiconductor die 52 and a substrate 64, such as a carrier substrate or an interposer (i.e., a flip-chip assembly 62) in a substantially vertical direction. In the sixth embodiment, at least one barrier 76 is disposed adjacent the periphery 51 of semiconductor die 52 and includes a space or opening 78 formed therein and configured to facilitate dispensing or injecting the resin 24 into a gap 72 between the semiconductor die 52 and the substrate 64. Further, as a dispenser 82 provides resin 24 through opening 78, the resin 24 preferably fills the gap 72 between the substrate 42 and

die 64 via capillary action, although positive or negative pressure may be applied to resin 24 as known in the art to accelerate the flow of resin 24 into the gap 72. As such, the at least one barrier 76 is provided to contain the resin in the gap 72 between the semiconductor die 52 and the substrate 64. Accordingly, as in the previous embodiments, it can be well appreciated that gravity provides a more uniform flow front 78, wherein the gravitational force induces the resin 24 to fill in spaces above solder bumps 66 where potential air pockets and/or voids are conventionally formed around the solder bumps 66 in the gap 72 between the substrate 42 and semiconductor die 64.

While the present invention has been disclosed in terms of certain preferred embodiments, those of ordinary skill in the art will recognize and appreciate that the invention is not so limited. Additions, deletions and modifications to the disclosed embodiments may be effected without departing from the scope of the invention as claimed herein. Similarly, features from one embodiment may be combined with those of another while remaining within the scope of the invention.

CLAIMS

What is claimed is:

1. A method of molding a semiconductor assembly in a mold cavity of a transfer mold comprising:

providing at least one substrate having at least one surface in said mold cavity; and

introducing a flowable material onto said at least one surface of said at least one substrate in an substantially vertical direction in said mold cavity.

2. The method according to claim 1, further comprising:

positioning said at least one substrate in at least one cavity of a transfer mold, said transfer mold having said at least one cavity substantially vertically oriented, said transfer mold including at least one gate at a lower portion of said at least one cavity and at least one vent at an upper portion thereof.

3. The method according to claim 2, wherein said introducing said flowable material comprises:

substantially filling said at least one cavity.

4. The method according to claim 3, wherein said filling said at least one cavity comprises:

introducing said flowable material through said at least one gate until a single flow front of said flowable material contacts said at least one vent at said upper portion of said cavity.

5. The method according to claim 2, wherein said positioning said at least one substrate further comprises:

positioning said at least one substrate substantially vertically.

6. The method according to claim 5, wherein said providing said flowable material comprises:

filling said at least one cavity until a single flow front of said flowable material contacts said at least one vent.

7. The method according to claim 6, wherein said filling said at least one cavity with said flowable material comprises:

encapsulating said at least one substrate.

8. The method according to claim 1, wherein said introducing said flowable material in said substantially vertical direction comprises:

inducing a substantially uniform flow front.

9. The method according to claim 1, wherein said introducing said flowable material comprises introducing said flowable material onto a substantially vertically oriented surface of said at least one substrate.

10. The method according to claim 1, wherein said introducing said flowable material onto at least one surface of said at least one substrate in said substantially vertical direction comprises:

substantially preventing voids in said flowable material.

11. The method according to claim 1, wherein said providing said at least one substrate comprises:

providing an assembly including said at least one substrate.

12. The method according to claim 11, wherein said providing said assembly comprises:

providing an assembly including at least one semiconductor die and a lead frame.

13. The method according to claim 11, wherein said providing said assembly comprises:

providing an assembly with said at least one substrate comprising at least one semiconductor die, said at least one semiconductor die being connected to a carrier including one of a carrier substrate and an interposer.

14. The method according to claim 13, wherein said providing said assembly comprises:

providing said assembly with said at least one semiconductor die spaced apart from said carrier.

15. The method according to claim 14, wherein said introducing comprises:

introducing said flowable material between said at least one semiconductor die and said carrier.

16. The method according to claim 1, wherein said providing said at least one substrate comprises:

providing at least one individual semiconductor die.

17. The method according to claim 16, wherein said providing said at least one individual semiconductor die comprises:

providing said at least one individual semiconductor die with conductive structure protruding therefrom.

18. The method according to claim 1, wherein said providing said at least one semiconductor die comprises:

providing a large-scale substrate including a plurality of semiconductor devices.

19. The method according to claim 18, wherein said providing said large-scale substrate comprises:

providing said large-scale substrate with conductive structures protruding from bond pads of said plurality of semiconductor devices.

20. The method according to claim 18, wherein said providing said large-scale substrate comprises:
providing at least a portion of a wafer.

21. The method according to claim 1, wherein said introducing includes capillary action acting on said flowable material.

22. The method according to claim 1, wherein said introducing includes positive pressure acting on said flowable material..

23. The method according to claim 1, wherein said introducing includes negative pressure acting on said flowable material.

24. The method according to claim 2, wherein at least a portion of said at least one cavity prevents said flowable material from covering bond pads of said at least one substrate.

25. The method according to claim 2, wherein said at least one cavity includes a cavity at least partially receiving conductive structures protruding from said at least one substrate and at least partially prevents said flowable material from covering said conductive structures.

26. A method of molding a semiconductor assembly in a mold cavity of a transfer mold comprising:
providing at least one substrate having at least one surface in said mold cavity; and
introducing a flowable material onto said at least one surface of said at least one substrate in an upward, substantially vertical direction in said mold cavity.

27. The method according to claim 26, further comprising:

positioning said at least one substrate in at least one cavity of a transfer mold, said transfer mold being configured with said at least one cavity substantially vertically oriented, said transfer mold including at least one gate at a lower portion of said at least one cavity and at least one vent at an upper portion thereof.

28. The method according to claim 27, wherein said introducing said flowable material comprises:

substantially filling said at least one cavity.

29. The method according to claim 28, wherein said filling said at least one cavity comprises:

introducing said flowable material through said at least one gate until a single flow front of said flowable material contacts said at least one vent at said upper portion of said cavity.

30. The method according to claim 27, wherein said positioning said at least one substrate further comprises:

positioning said at least one substrate substantially vertically.

31. The method according to claim 30, wherein said providing said flowable material comprises:

filling said at least one cavity until a single flow front of said flowable material contacts said at least one vent.

32. The method according to claim 31, wherein said filling said at least one cavity with said flowable material comprises:

encapsulating said at least one substrate.

33. The method according to claim 26, wherein said introducing said flowable material in said non-horizontal direction comprises:
inducing a substantially uniform flow front.

34. The method according to claim 26, wherein said introducing said flowable material flows substantially across said surface of said at least one substrate.

35. The method according to claim 26, wherein said introducing said flowable material onto at least one surface of said at least one substrate in said non-horizontal direction comprises substantially preventing voids in said flowable material.

36. The method according to claim 26, wherein said providing said at least one substrate comprises:
providing an assembly including said at least one substrate.

37. The method according to claim 36, wherein said providing said assembly comprises:
providing an assembly including at least one semiconductor die and a lead frame.

38. The method according to claim 36, wherein said providing said assembly comprises:
providing an assembly with said at least one substrate including at least one semiconductor die, said at least one semiconductor die being connected to a carrier including one of a carrier substrate and an interposer.

39. The method according to claim 38, wherein said providing said assembly comprises:
providing said assembly with said at least one semiconductor die being spaced apart from said carrier.

40. The method according to claim 39, wherein said introducing comprises:
introducing said flowable material between said at least one semiconductor die and said carrier.

41. The method according to claim 26, wherein said providing said at least one substrate comprises:
providing at least one individual semiconductor die.

42. The method according to claim 41, wherein said providing said at least one individual semiconductor die comprises:
providing said at least one individual semiconductor die with conductive structure protruding therefrom.

43. The method according to claim 26, wherein said providing said at least one semiconductor die comprises:
providing a large-scale substrate including a plurality of semiconductor devices.

44. The method according to claim 43, wherein said providing said large-scale substrate comprises:
providing said large-scale substrate having conductive structures protruding from bond pads of said plurality of semiconductor devices.

45. The method according to claim 44, wherein said providing said large-scale substrate comprises:
providing at least a portion of a wafer.

46. The method according to claim 26, wherein said introducing includes capillary action on said flowable material.

47. The method according to claim 26, wherein said introducing includes positive pressure on said flowable material.

48. The method according to claim 26, wherein said introducing includes negative pressure on said flowable material.

49. The method according to claim 27, wherein said at least one cavity includes a portion preventing said flowable material from covering bond pads of said at least one substrate.

50. The method according to claim 27, wherein said at least one cavity includes at least a portion thereof partially receiving conductive structures protruding from said at least one substrate and partially preventing said flowable material from covering said conductive structures.

51. A molding method for a substrate in a transfer mold having at least one cavity, the method comprising:
providing at least one substrate; and
introducing a flowable material onto at least one surface of said at least one substrate in an upward, non-horizontal direction in said cavity.

52. The method according to claim 51, further comprising:
positioning said at least one substrate in said at least one cavity of said transfer mold, said transfer mold having said at least one cavity non-horizontally oriented and including at least one gate at a lower portion of said at least one cavity and at least one vent at an upper portion thereof.

53. The method according to claim 52, wherein said introducing said flowable material comprises:
substantially filling said at least one cavity.

54. The method according to claim 53, wherein said filling said at least one cavity comprises:

introducing said flowable material through said at least one gate until a single flow front of said flowable material contacts said at least one vent at said upper portion of said cavity.

55. The method according to claim 52, wherein said positioning said at least one substrate further comprises:

positioning said at least one substrate substantially vertically.

56. The method according to claim 55, wherein said providing said flowable material comprises:

filling said at least one cavity until a single flow front of said flowable material contacts said at least one vent.

57. The method according to claim 56, wherein said filling said at least one cavity with said flowable material comprises:

encapsulating said at least one substrate.

58. The method according to claim 51, wherein said introducing said flowable material in said non-horizontal direction comprises:

inducing a substantially uniform flow front.

59. The method according to claim 51, wherein said introducing said flowable material flows onto a substantially vertically oriented surface of said at least one substrate.

60. The method according to claim 51, wherein said introducing said flowable material onto at least one surface of said at least one substrate in said non-horizontal direction comprises:

substantially preventing voids in said flowable material.

61. The method according to claim 51, wherein said providing said at least one substrate comprises:

providing an assembly including said at least one substrate.

62. The method according to claim 61, wherein said providing said assembly comprises:

providing an assembly including at least one semiconductor die and a lead frame.

63. The method according to claim 61, wherein said providing said assembly comprises:

providing an assembly with said at least one substrate including at least one semiconductor die, said at least one semiconductor die being connected to a carrier including one of a carrier substrate and an interposer.

64. The method according to claim 63, wherein said providing said assembly comprises:

providing said assembly with said at least one semiconductor die being spaced apart from said carrier.

65 The method according to claim 61, wherein said flowable material flows between said at least one semiconductor die and saidcarrier.

66. The method according to claim 51, wherein said providing said at least one substrate comprises:

providing at least one individual semiconductor die.

67. The method according to claim 66, wherein said providing said at least one individual semiconductor die comprises:

providing said at least one individual semiconductor die with conductive structure protruding therefrom.

68. The method according to claim 51, wherein said providing said at least one semiconductor die comprises:

providing a large-scale substrate including a plurality of semiconductor devices.

69. The method according to claim 68, wherein said providing said large-scale substrate comprises:

providing said large-scale substrate with conductive structures protruding from bond pads of said plurality of semiconductor devices.

70. The method according to claim 68, wherein said providing said large-scale substrate comprises:

providing at least a portion of a wafer.

71. The method according to claim 51, wherein said introducing includes capillary action acting on said flowable material.

72. The method according to claim 51, wherein said introducing includes positive pressure on said flowable material.

73. The method according to claim 51, wherein said introducing includes negative pressure on said flowable material.

74. The method according to claim 52, wherein said at least one cavity prevents said flowable material from covering bond pads of said at least one substrate.

75. The method according to claim 52, wherein a portion said at least one cavity at least partially receives conductive structures protruding from said at least one substrate and at least partially prevents said flowable material from covering said conductive structures.

76. A method for transfer molding at least one semiconductor device component, the method comprising:

providing at least one transfer mold having at least one cavity, said at least one cavity including at least one gate at a lower portion thereof and at least one vent at an upper portion thereof;

positioning at least one substrate within said at least one cavity; and

introducing a resin material into said at least one cavity through said at least one gate so that said resin material moves upwardly over said at least one substrate in a non-horizontal direction.

77. The method according to claim 76, comprising:

removing substantially all gas within said cavity therefrom through said at least one vent during said introducing.

78. The method according to claim 76, wherein said introducing comprises:

encapsulating said at least one substrate.

79. The method according to claim 76, wherein said providing said at least one transfer mold comprises:

providing a transfer mold with said at least one cavity being oriented non-horizontally.

80. The method according to claim 29, wherein said providing said at least one transfer mold comprises:

providing said at least one transfer mold with said at least one cavity being substantially vertically oriented.

81. The method according to claim 76, wherein said introducing includes a single, substantially uniform flow front around said at least one substrate.

82. The method according to claim 76, wherein said introducing includes introducing flowable material until a single, substantially uniform flow front of said resin material contacting said at least one vent at an upper portion of said at least one cavity.

83. The method according to claim 76, wherein said providing said at least one substrate comprises:
providing at least one semiconductor device connected to a lead frame.

84. The method according to claim 76, wherein said providing said at least one substrate comprises:
providing an assembly including a semiconductor device and a carrier comprising one of a carrier substrate and an interposer.

85. The method according to claim 84, wherein said providing said assembly comprises:
providing an assembly including a flip chip type semiconductor device.

86. The method according to claim 84, wherein said providing said assembly comprises:
providing said assembly with said semiconductor device being spaced apart from said carrier.

87. The method according to claim 86, wherein said introducing comprises:
introducing said resin material between said semiconductor device and said carrier.

88. The method according to claim 37, wherein said introducing further comprises:

at least partially encapsulating at least one of said semiconductor device and said carrier.

89. The method according to claim 76, wherein said providing said at least one transfer mold comprises:

providing at least one transfer mold having a cavity surface including protrusions disposed against contact pads of said at least one substrate.

90. The method according to claim 76, wherein said providing said at least one transfer mold comprises:

providing at least one transfer mold with a cavity surface including recesses therein at least partially receiving conductive structures protruding from said at least one substrate.

91. A transfer molding apparatus comprising:

first and second members configured to be assembled with one another;

at least one cavity formed in at least one of said first and second members, said cavity substantially non-horizontally oriented during a transfer molding process;

at least one gate at a lower portion of said at least one cavity; and

at least one vent at an upper portion of said at least one cavity.

92. The apparatus according to claim 91, wherein said at least one cavity comprises a substantially vertically oriented cavity.

93. The apparatus according to claim 91, wherein said at least one cavity includes at least one surface with recesses formed therein, said recesses at least partially receiving conductive structures protruding from a substrate upon positioning of said substrate within said at least one cavity.

94. The apparatus according to claim 91, wherein said at least one cavity includes at least one surface with protrusions disposed against contact pads of a substrate.

95. A transfer molding apparatus comprising:

first and second members to be assembled with one another;

at least one cavity formed in at least one of said first and second members, said cavity oriented substantially vertically for a transfer molding process;

at least one gate at a lower portion of said at least one cavity; and

at least one vent at an upper portion of said at least one cavity.

96. The apparatus according to claim 95, wherein said at least one cavity includes a substantial vertically flow of a molding material during a transfer molding process.

97. The apparatus according to claim 95, wherein said at least one cavity includes at least one surface with recesses formed therein, said recesses including portions receiving conductive structures protruding from a substrate upon positioning of said substrate within said at least one cavity.

98. The apparatus according to claim 95, wherein said at least one cavity includes at least one surface with protrusions for engaging portions of contact pads of a substrate.

ABSTRACT OF THE DISCLOSURE

A method and apparatus for reducing or eliminating the formation of air pockets or voids in a flowable material provided in contact with at least one substrate. The flowable material is provided in a non-horizontal direction, and flows from a lower position to an upper position. As a result, the flowable material is provided uniformly with a single, uniform flow front due to gravity acting thereon and gravity, thereby, substantially prevents voids and air pockets from forming in the flowable material. In one embodiment, the at least one substrate is provided in the cavity of a transfer mold, in which the cavity is filled from a gate at a lower portion of the cavity to a vent at an upper portion of the cavity. In another embodiment, a bumped semiconductor device is attached to a substrate having a gap therebetween, in which the gap is oriented longitudinally perpendicular to a horizontal plane so that the flowable material may feel the gap in a vertical direction.

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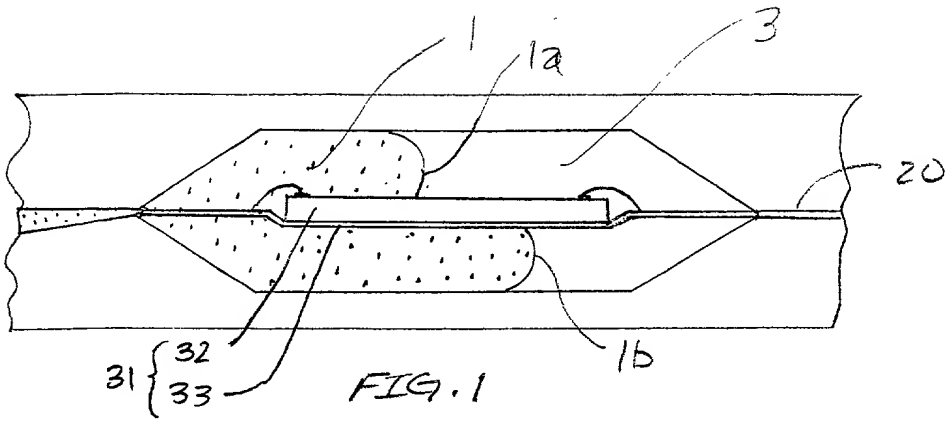

FIG. 1

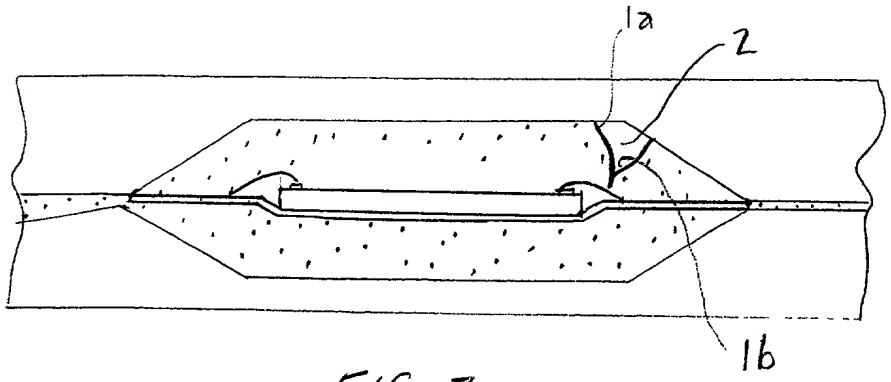

FIG. 2

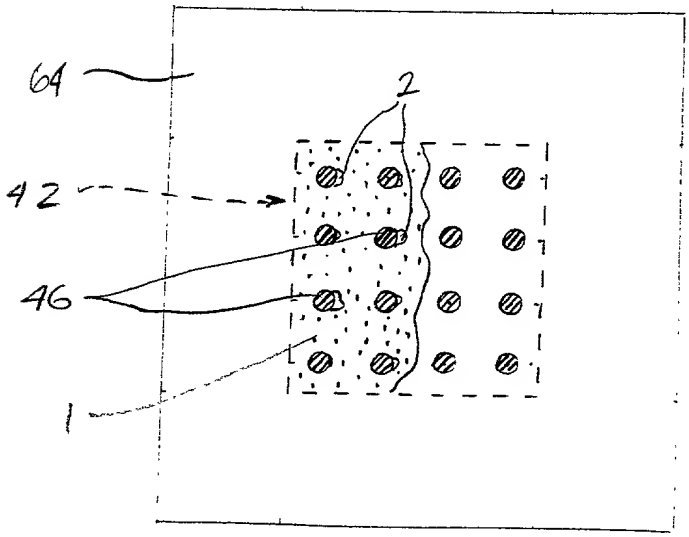

FIG. 3

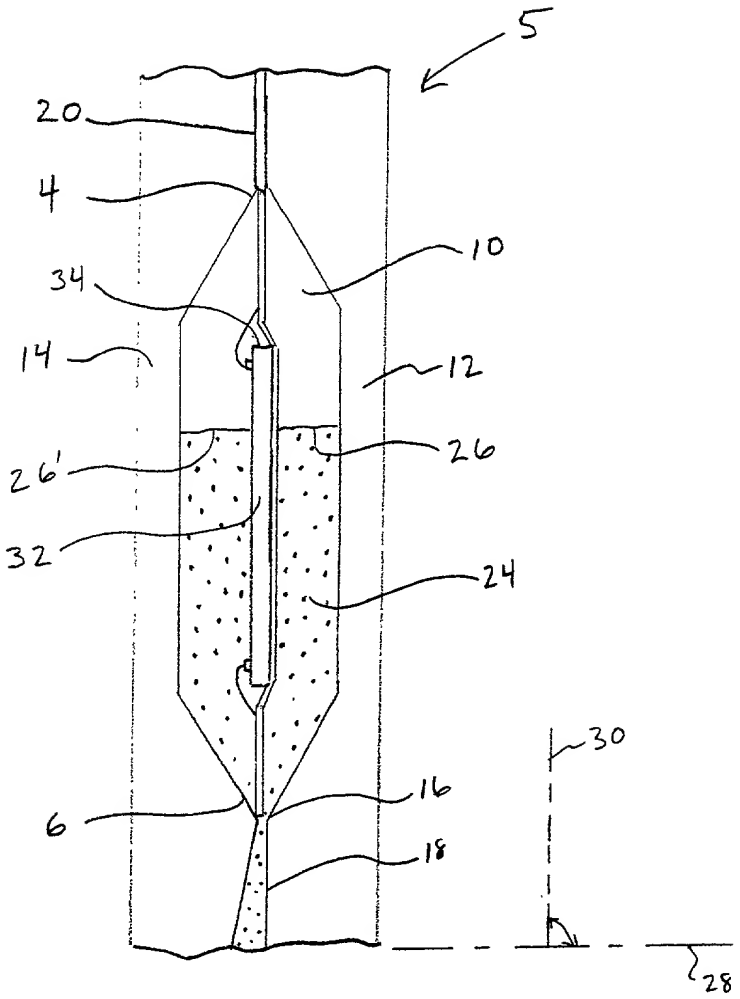

FIG. 4

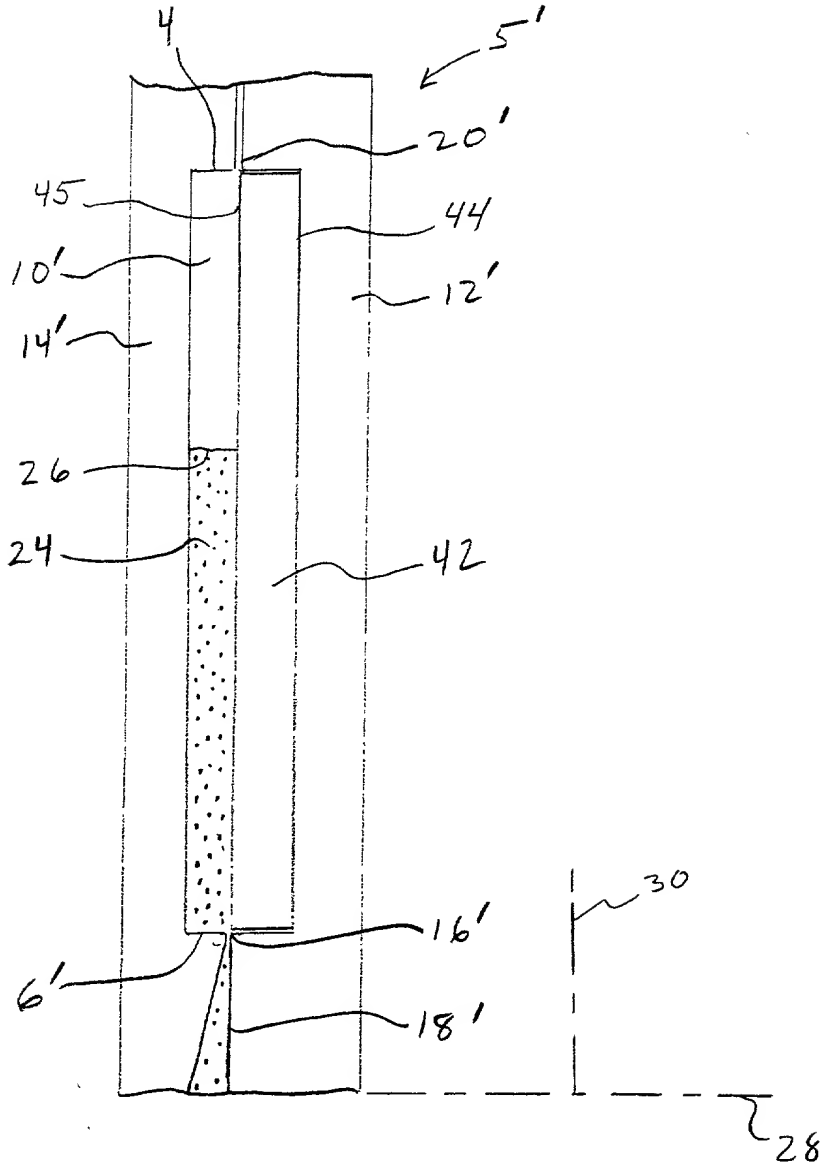

FIG. 5

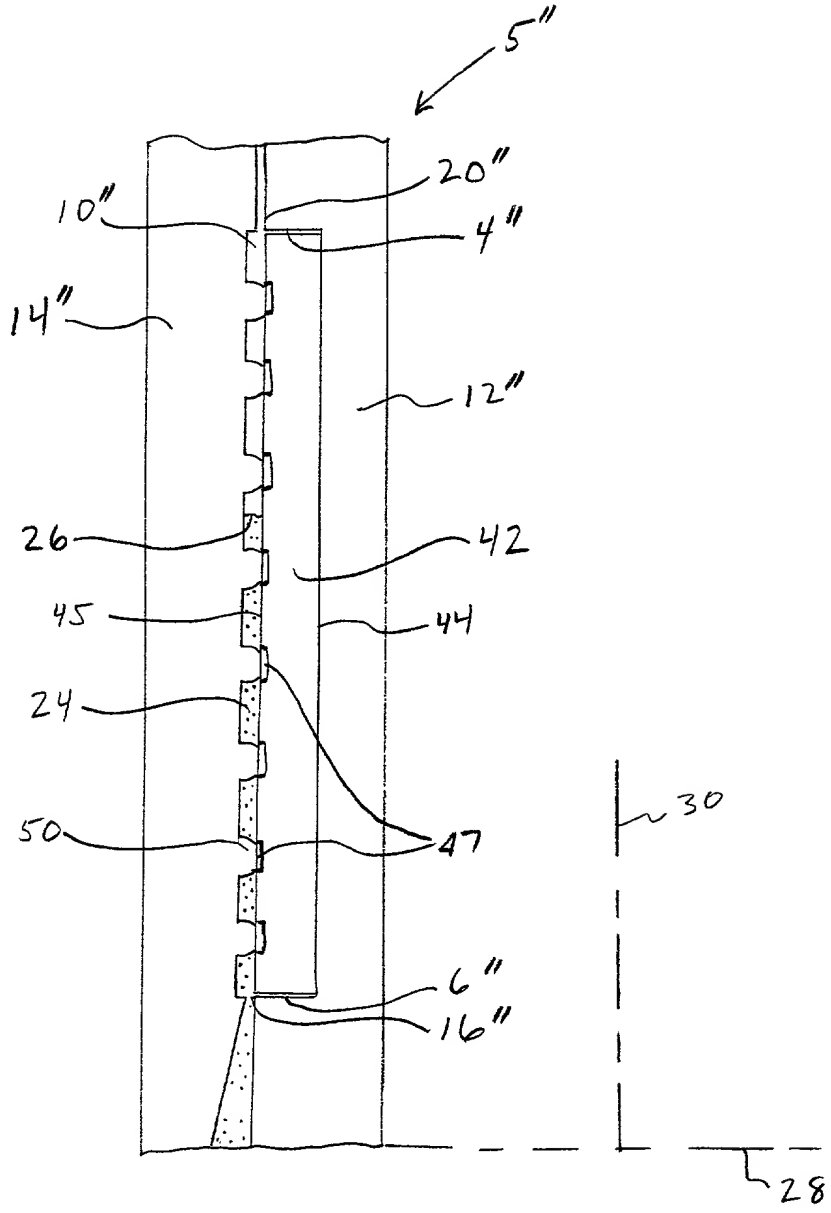

FIG. 6

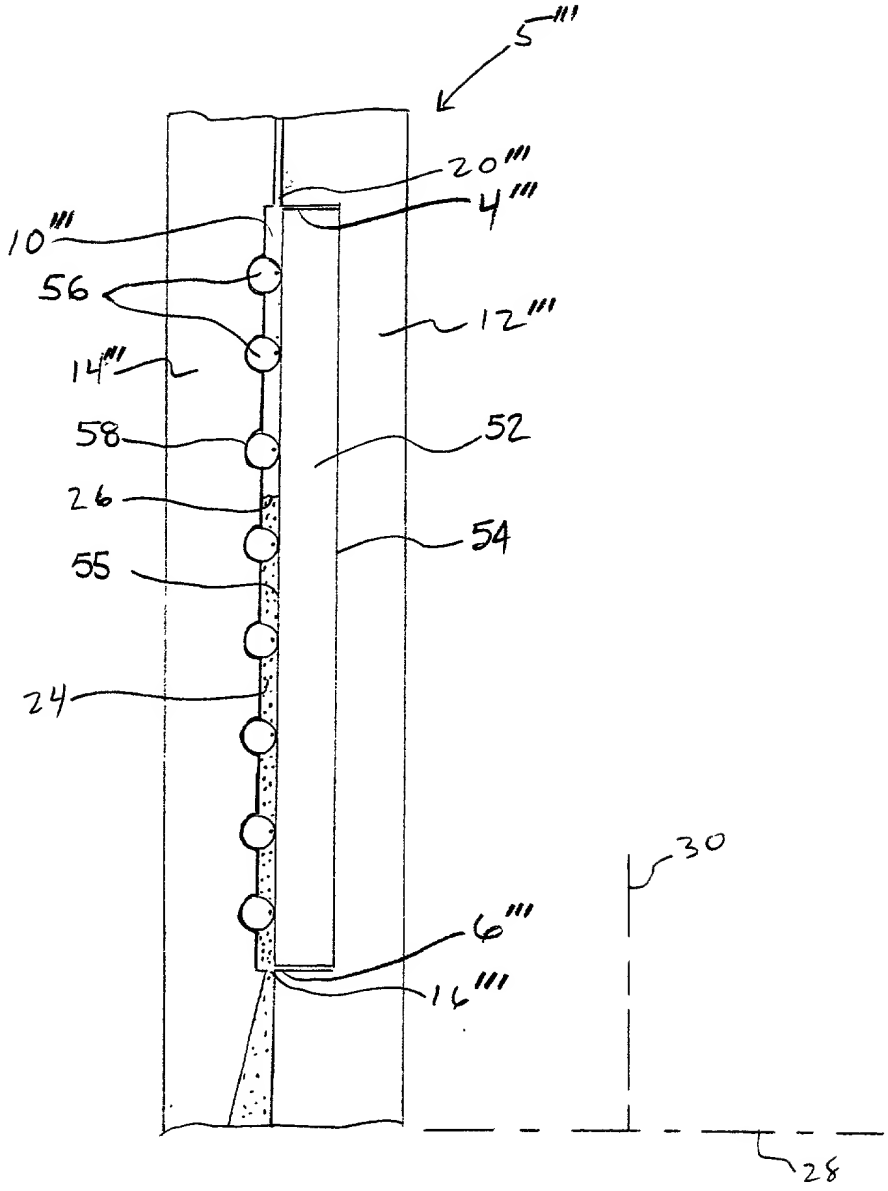

FIG. 7

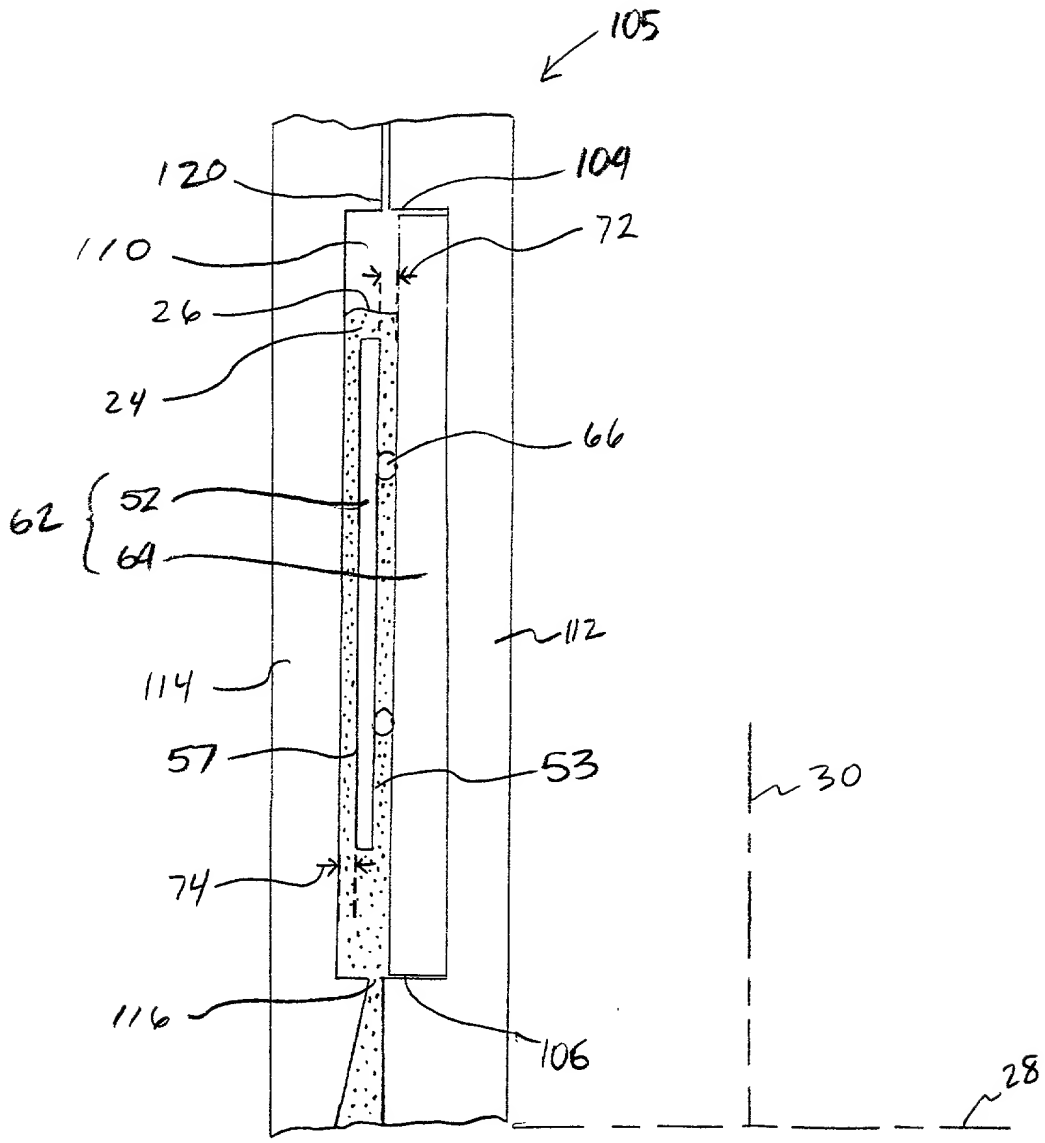

FIG. 8

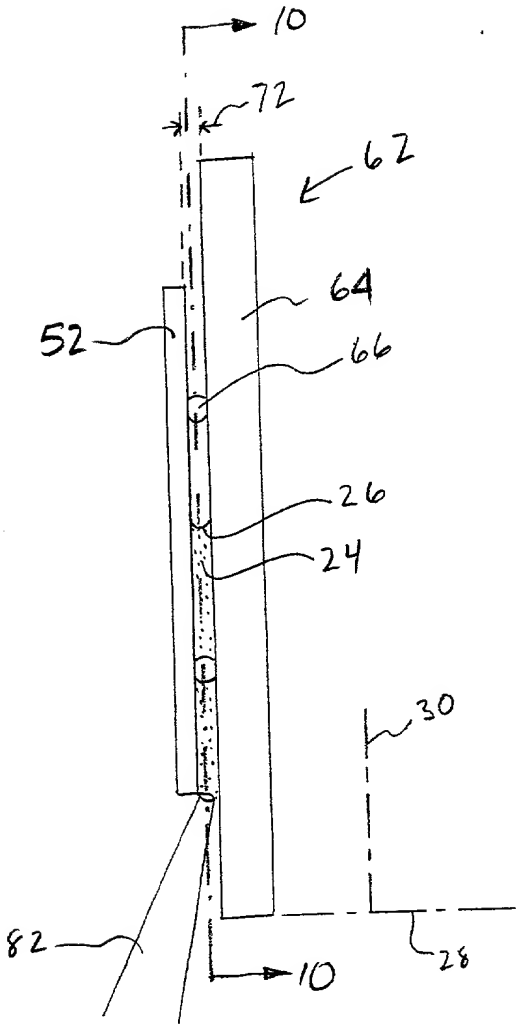

FIG. 9

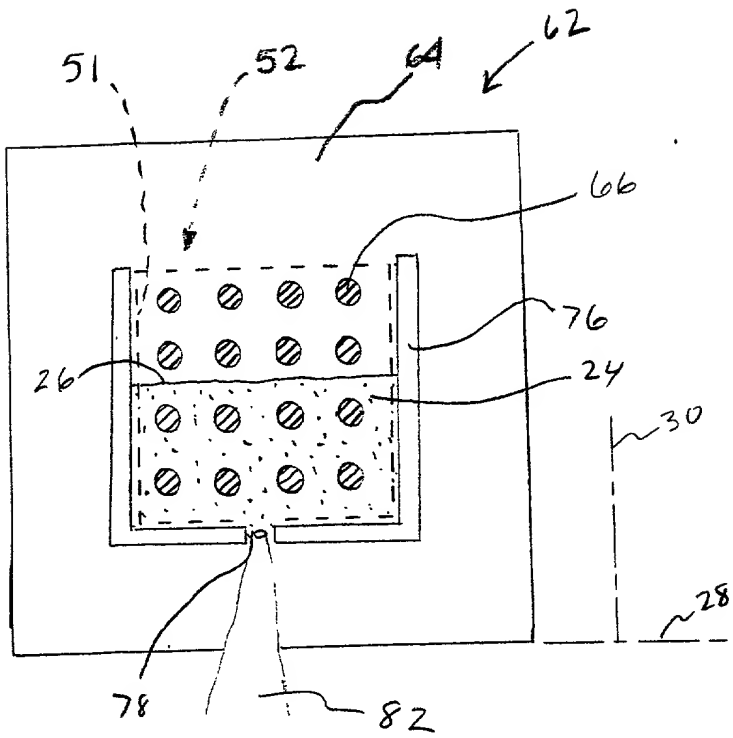

FIG. 10

DECLARATION FOR PATENT APPLICATION (WITH POWER OF ATTORNEY)

As an inventor named below or on any attached continuation page, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled TRANSFER MOLDING AND UNDERFILLING METHOD AND APPARATUS, the specification of which (check one):

- ☒ is attached hereto.
- ☐ was filed on _____ as United States application serial no. _____ and was amended on _____.
- ☐ was filed on _____ as PCT international application no. _____ and was amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT international application(s) designating at least one country other than the United States of America listed below and on any attached continuation page and have also identified below and on any attached continuation page any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America having a filing date before that of the application(s) on which priority is claimed.

Prior foreign/PCT application(s):

			Priority Claimed	
(number)	(country)	(day/month/year filed)	Yes	No
(number)	(country)	(day/month/year filed)	Yes	No

☐ I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or § 365(c) of PCT international application(s) designating the United States of America listed below and on any attached continuation page and, insofar as the subject matter of each of the claims of this application is not disclosed in any such prior application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of such prior application and the national or PCT international filing date of this application:

(application serial no.)	(filing date)	(status - pending, patented or abandoned)
(application serial no.)	(filing date)	(status - pending, patented or abandoned)

☐ I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

(provisional application no.)	(filing date)

I hereby appoint the following Registered Practitioners to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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Salt Lake City, Utah 84110

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's signature _____ Date _____
Residence: Meridian, Idaho
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